INTERNATIONAL CONFERENCE ON RESEARCHES IN ENGINEERING, SCIENCE, TECHNOLOGY, MANAGEMENT AND HUMANITIES (ICRESTMH – 2024)

25TH AUGUST, 2024

CERTIFICATE NO : ICRESTMH /2024/C0824880

A Study of VLSI Technologies for Implementing Low Power MAC Units

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ABSTRACT

Very-Large-Scale Integration (VLSI) technologies play a crucial role in implementing low-power Multiply–Accumulate (MAC) units, which are fundamental building blocks in digital signal processing (DSP), image processing, and machine learning accelerators. As modern portable and battery-operated devices demand high performance with minimal energy consumption, the design of low-power MAC units has become a primary objective in VLSI system design. Advanced CMOS scaling technologies enable reduced supply voltage and smaller transistor sizes, thereby lowering dynamic and static power dissipation. Techniques such as clock gating, power gating, operand isolation, and dynamic voltage and frequency scaling (DVFS) are widely employed to minimize switching activity and leakage currents in MAC architectures. Furthermore, the use of efficient multiplier architectures like Booth multipliers, Wallace tree multipliers, and compressor-based adders significantly reduces propagation delay and power consumption. Pipelining and parallelism are also incorporated to optimize throughput while maintaining energy efficiency. Emerging technologies such as FinFETs and near-threshold computing further enhance low-power performance in deep submicron regimes. Additionally, approximate computing techniques are increasingly adopted in error-tolerant applications to reduce hardware complexity and energy usage.